CLAIMS:

1. A data carrier (4) for the transfer of communication data (KD1, KD2) via at least two interface means (11, 12) having
first interface means (11) for receiving a first communication signal (KS1), and having
second interface means (12) for receiving a second communication signal (KS2), and having
processing means (13) to which a first clock signal (TS1) derived from the first communication signal (KS1) or a second clock signal (TS2) derived from the second communication signal (KS2) can be applied for the processing of the transferred communication data (KD1, KD2), and having
reset means (21) for resetting the processing by the processing means (13),
characterized in that
a first frequency sensor (22) is included, which is adapted to supply first frequency reset information (RI4) to the reset means (21) when a first clock frequency of the first clock signal (TS1) or the frequency (FKS1) of the first communication signal (KS1) lies below a first lower frequency threshold (FU1), and
a second frequency sensor (23) is included, which is adapted to supply second frequency reset information (RI5) to the reset means (21) when a second clock frequency of the second clock signal (TS2) or the frequency (FKS2) of the second communication signal (KS2) lies below a second lower frequency threshold (FU2), and
the reset means (21) are adapted to reset the processing by the processing means (13) when the first clock signal (TS1) is applied to the processing means (13) and the first frequency reset information (RI4) is received or when the second clock signal (TS2) is applied to the processing means (13) and the second frequency reset information (RI5) is received.

2. A data carrier (4) as claimed in claim 1, characterized in that the first frequency sensor (22) is adapted to supply the first frequency reset information (RI4) to the reset means (21) when the first clock frequency or the frequency (FKS1) of the first communication signal (KS1) lies above a first upper frequency threshold (FO1), and the second frequency sensor (23) is adapted to supply the second frequency reset information (RI5) to the reset means (21) when the second clock frequency or the frequency (FKS2) of

the second communication signal (KS2) lies above a second upper frequency threshold (FO2).

3. A data carrier (4) as claimed in claim 1, characterized in that clock generation means (19) are included, which means are adapted to generate an internal clock signal (TS3) having a third clock frequency, and the reset means (21) are adapted to reset the processing by the processing means (13) when the third clock signal (TS3) is applied to the processing means (13) and both the first frequency reset information (RI4) and the second frequency reset information (RI5) are applied to the reset means (21).

4. A data carrier (4) as claimed in claim 3, characterized in that clock generation means (19) are included, which means are adapted to generate the internal clock signal (TS3) having the third clock frequency, and the reset means (21) are adapted to inhibit the resetting of the processing by the processing means (13) when the third clock signal (TS3) is applied to the processing means (13) and the first frequency reset information (RI4) and/or the second frequency reset information (RI5) is applied to the reset means (21).

5. A data carrier as claimed in claim 1, characterized in that a first clock derivation stage is adapted to derive the first clock signal from the first communication signal and the first frequency sensor is adapted to apply the first frequency reset information to the first clock derivation stage when the first clock frequency of the first clock signal is below the first frequency threshold, the clock derivation stage being adapted to change the derivation of the first clock signal when the first frequency reset information is received.

6. A data carrier (4) as claimed in claim 1, characterized in that the data carrier (4) takes the form of an integrated circuit.